

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 08-181983

(43)Date of publication of application : 12.07.1996

(51)Int.Cl.

H04N 7/24

H03M 7/00

H03M 13/00

(21)Application number : 06-317929

(71)Applicant : OKI ELECTRIC IND CO LTD

(22)Date of filing : 21.12.1994

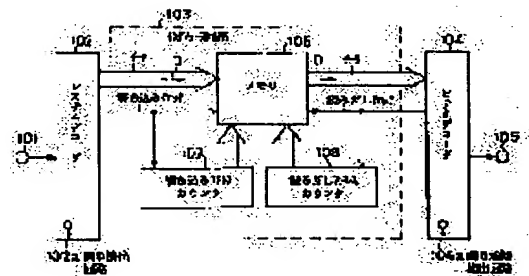
(72)Inventor : NAKAI TOSHIHISA
MATSUMURA YASUKO

(54) IMAGE DECODING CIRCUIT

(57)Abstract:

PURPOSE: To realize decoding with a very simple configuration and excellent image quality when a data error is included in received moving image coding data.

CONSTITUTION: A system decoder 102 has an error check circuit 102a comprising a microprocessor or the like in the inside and decodes packet data received from an input terminal 101 and provides an output of an error notice unique word when a data error is checked. When no data error is detected, a pay load is given to a video decoder 104 via an interface circuit 103. The video decoder 104 is provided with an error notice check circuit 104a comprising a microprocessor or the like to control an internal video decoder. The video decoder 104 provides an output of decoded image data to an output terminal 105.



LEGAL STATUS

[Date of request for examination]

12.02.1998

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

2898212

[Date of registration]

12.03.1999

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]